Core Layer 3 Switch 100G Port Channel Link Balancing Technical Notes - Official Technical Overview & Hardware Datasheet

EXECUTIVE SUMMARY

The Core Layer 3 Switch 100G Port Channel Link Balancing Technical Notes platform represents the pinnacle of high-density, carrier-class routing silicon designed for next-generation datacenter and campus core fabrics. This document provides an authoritative technical deep-dive into the hardware architecture, firmware logic, and algorithmic balancing mechanisms that enable line-rate 100G forwarding with deterministic low latency and sub-microsecond jitter across aggregated Port Channel (LAG) interfaces.

Engineered for the most demanding spine-leaf and collapsed-core topologies, this platform integrates a non-blocking switching fabric with an advanced hash engine that performs per-packet and per-flow load distribution across up to 32 member links. The system is purpose-built to eliminate micro-burst congestion, optimize buffer utilization, and ensure symmetrical traffic distribution across 100G Ethernet Port Channels.



HARDWARE ARCHITECTURE & SILICON

The system is anchored by a fifth-generation programmable forwarding ASIC, fabricated on a 7nm process node, delivering 12.8 Tbps of full-duplex switching capacity in a compact 1RU form factor. The silicon integrates 128 lanes of 100G PAM4 SerDes, enabling native 100G and breakout 4x25G or 4x10G operation without external PHY retimers.

The ASIC's traffic manager employs a three-stage hierarchical queuing engine with 64 MB of shared packet buffer, dynamically partitioned across eight traffic classes. A dedicated Port Channel Hash Engine (PCHE) operates in parallel with the main forwarding pipeline, executing a configurable 5-tuple or 7-tuple hash on every ingress frame. The PCHE supports dynamic load balancing based on link utilization feedback, a mechanism that prevents hash polarization in large

LAG groups.

KEY FEATURES & ROUTING LOGIC

- Port Channel Link Balancing: Hardware-assisted per-packet and per-flow hashing with adjustable polynomial selection, enabling deterministic distribution across 32 x 100G member links.
- Dynamic Load Rebalancing: Real-time link utilization monitoring with sub-millisecond rebalancing decisions to mitigate flow collisions and micro-bursts.
- Non-Blocking Architecture: Full line-rate forwarding on all ports simultaneously with zero head-of-line blocking.
- Advanced QoS: 8 priority queues per port, WRED, and strict priority scheduling with egress shaping at 100G granularity.
- Resilient L3 Routing: OSPF, BGP, IS-IS, and RIP with hardware-accelerated route lookup and 1M IPv4 / 512K IPv6 forwarding entries.
- VXLAN/EVPN Overlay: Native VXLAN-GPE termination with 4K tunnels and EVPN Type-2/Type-3 route support.
- Redundancy: Dual hot-swappable AC/DC power supplies and redundant fan trays with N+1 fan redundancy.

COMPLIANCE & STANDARDS

The Core Layer 3 Switch 100G Port Channel Link Balancing Technical Notes platform conforms to the following industry standards and regulatory directives:

- IEEE 802.3ba (40G/100G Ethernet), IEEE 802.3cd (50G/100G), IEEE 802.1AX-2020 (Link Aggregation)
- IEEE 802.1Q (VLAN), 802.1ad (QinQ), 802.1p (QoS), 802.3x (Flow Control)
- IEEE 802.1BR (Port Extender), 802.1Qbg (Edge Virtual Bridging)
- IETF RFC 7432 (EVPN), RFC 7348 (VXLAN), RFC 4271 (BGP-4), RFC 2328 (OSPFv2)
- MEF 3.0, MEF 10.3, MEF 6.2
- RoHS-6, WEEE, REACH, UL 60950-1, IEC 60950-1, EN 55032 Class A, EN 55024, FCC Part 15 Subpart B Class A

TECHNICAL SPECIFICATIONS

Parameter	**Specification**
Form Factor	1RU Fixed Configuration, 19-inch Rack Mountable
Switching Capacity	12.8 Tbps Full-Duplex, Non-Blocking
Forwarding Rate	9.5 Bpps (64-byte packets, line rate)

Port Channel Support	Up to 128 LAG groups, 32 members per group, 100G per member
Hash Algorithm	Configurable 5-tuple/7-tuple, dynamic load balancing, per-packet and per-flow modes
Packet Buffer	64 MB Shared, 8 Traffic Classes, WRED
Power Supply	Dual Hot-Swappable Redundant AC/DC, 1600W Each, N+1 Fan Redundancy
Airflow	Front-to-Back or Back-to-Front, Field-Reversible
Operating Temperature	0 ° C to 40 ° C (32 ° F to 104 ° F), Short-Term -5°C to 55°C
MTBF	> 350,000 Hours
Management	CLI, SNMPv3, NETCONF/YANG, RESTCONF, Syslog, TACACS+, RADIUS
Latency	< 1.2 µs Port-to-Port (100G, 64-byte)
L3 Routing Table	1M IPv4 / 512K IPv6 Forwarding Entries
VXLAN Tunnels	4K VXLAN-GPE Tunnels, EVPN Type-2/Type-3
Compliance	IEEE 802.3ba/cd, 802.1AX, 802.1Q, MEF

	3.0, RoHS-6, UL 60950-1

ORDERING SKU INFORMATION

- SKU-CLS-100G-48Y: 48x100G QSFP28 + 8x400G QSFP-DD, dual AC PSU
- SKU-CLS-100G-32C: 32x100G QSFP28 + 2x10G SFP+, dual DC PSU
- SKU-CLS-100G-16C: 16x100G QSFP28 + 4x25G SFP28, dual AC PSU
- SKU-CLS-100G-FAN: Spare fan tray, N+1 redundant
- SKU-CLS-100G-PWR-AC: Spare 1600W AC power supply
- SKU-CLS-100G-PWR-DC: Spare 1600W DC power supply

